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COMPUTER-AIDED DESIGN AND PROGRAMMING

Elmor Model-based Algorithm to Select Optimal Connections on the Clock Tree[1]

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Abstract—Consideration was given to two formulations of the problem of selecting the optimal types of interconnections on the edges of the given rooted tree along which the signal is transmitted from the root to the terminals. The time interval during which the signal must be received was defined for each terminal. The time of signal propagation which depends on the interconnections used on all tree edges was calculated using the Elmor formulas. It was required to select interconnections of the minimal total capacitance such that the times of signal arrival to each terminal be admissible. Pseudopolynomial algorithms of dynamic programming were proposed to determine optimal solutions of the examined problems.

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1. INTRODUCTION

The time of signal propagation is one of the main characteristics of efficiency of the modern very large-scale integrated (VLSI) circuits [1]. The integrated circuits consist of multiple networks containing each special vertices that are called the *terminals*. Since the terminals make up part of the VLSI circuits, the instants of arrivals of the signal sent along the *clock tree* may be defined for each terminal with the aim of coordinating the entire circuit. The most general case is represented by assigning to each terminal the time interval during which the signal should be received.

For prompt estimation of the signal propagation time in the VLSI circuits, the Elmor model is used as a rule [2]. Although the Elmor formulas enable one to calculate efficiently the signal propagation time over a tree with interconnections of certain types [3], the choice of the *optimal* types of interconnections is an NP-hard problem [4].

Let the capacitance $c_{ij}(x)$ and resistance $r_{ij}(x)$ of the edge (i, j) be defined by functions depending on the type x of the interconnection used. Since these characteristics are independent of direction, we use the term "edge" wherever the arc orientation is of no concern.

In the existing publications, the choice of interconnections on the edges of a given clock tree is usually confined to determination of their width. This subject matter is considered in a number of

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publications [1, 4–11] that are reviewed in detail in [4, 12]. For example, an algorithm to minimize the linear convolution of the times of signal arrivals to the terminals by selecting an optimal wire size of interconnections was proposed in [1]. It relies on the ideas of dynamic programming (DP) and constructs the optimal solution with an exponential complexity $O(n^X)$, where n is the number of the tree vertices and X is the number of permissible dimensions of interconnections.

Apart from selection of the wire size, other characteristics are examined in the publications. For example, a two-parameter DP algorithm determining the wire size and buffer insertion for a special case of the resistance and capacitance functions like

$$r_{ij}(x) = \frac{rl_{ij}}{x}; \quad c_{ij}(x) = cl_{ij}x, \tag{1}$$

where l_{ij} is the length of the edge (i, j) and r and c are the given nonnegative constants (specific resistance and specific capacitance), was proposed in [5]. In terms of the above notation, the algorithm determines the optimal wire size for a special case of the problem of complexity $O(n^2X^2)$. The problem of minimization of the time of signal transmission by selecting buffers and their size, as well as the wire size for the case where the width takes on continuous values from the given interval was solved analytically in [10]. The coupling capacitance was taken into account in [4, 11] at selecting the wire size. In [12], the problems and results related with the choice of interconnection types were reviewed, and a new methodology of selecting the wire size with simultaneous minimization of both the signal transmission time and the crosstalk noise was proposed. The so-defined multicriteria problem comes to determination of the Nash equilibrium.

The present paper considers a sufficiently general formulation of the problem of selecting the interconnection types for the case of arbitrary functions of capacitance, $c_{ij}(x)$, and resistance, $r_{ij}(x)$, of the edges (i, j). The interconnections having the least total capacitance and assuring timely arrival of the signal to all terminals of the clock tree are sought at that. A *one-parameter* DP algorithm of complexity $O(nXD^2)$, where D is the maximum admissible time of signal propagation from the tree root to the terminals and X is the maximum number of interconnection types that may be used on one edge, was proposed to solve this problem.

Consideration also was given to a special case of the problem where it is required to select the interconnection *width* if the edge resistance and capacitance obey (1). In this case, the complexity of the proposed algorithm is bounded by $O(nXD\min\{nX, D\})$.

A number of heuristic algorithms to construct a *planar* Steiner tree having one or another property on the rectangular lattice has been developed. Yet the networks of the VLSI circuits are placed in a three-dimensional lattice, rather than on a plane. At that, in one layer interconnections of a single type are often used. With regard for the aforementioned and the steady growth in the number of IC layers, of interest is the second problem which lies in determining the placement layer for each arc of the planar tree. In this case, the type of interconnection is the number of the layer where the arc is placed. This problem is not a special case of the preceding one. For the arbitrary interconnection cost functions, an algorithm of complexity $O(ND^4)$ is suggested for its solution, where N is the number of the planar tree vertices. To our knowledge, this is the first pseudopolynomial algorithm determining the optimal solution of this problem. Intermediate results were published in [13, 14].

2. FORMULATION OF THE PROBLEM

In the present paper we use the following Elmor formulas [2] which commonly are employed for an effortless estimation of the signal propagation times in the current-day VLSI circuits. Let given be the tree $T = (V, E)$ with the vertex set $V = \{0, 1, \ldots, n\}$, subset of terminals $V' \subseteq V\backslash\{0\}$, and set of E arcs directed from the root. The root vertex 0 is the source of signal. We denote

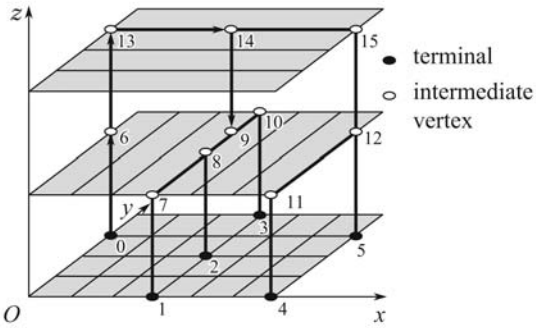

Fig. 1. Example of tree in the three-layered graph.

by P_k the path from the root to the vertex k; T_i is the subtree with the root at the vertex $I \in V$; r_{ij} is the resistance of the arc $(i,j) \in E$; c_{ij} is the capacitance of the arc $(i,j) \in E$; r_0 is the resistance at the root; c_i is the capacitance of the vertex $i \in V\backslash\{0\}$; and $C_j = \sum\limits_{(u,v)\in T_j} c_{uv} + \sum\limits_{u\in T_j} c_u$ is the total capacitance of the subtree T_j, $j \in V$.

Then, the time of signal propagation (delay) along the arc (i,j) is as follows:

$$d_{ij} = r_{ij}(c_{ij}/2 + C_j), \tag{2}$$

and the time of signal propagation from the root to the vertex $k \in V$ (delay to k) obeys the formula

$$t_k = r_0 C_0 + \sum_{(i,j)\in P_k} d_{ij}. \tag{3}$$

Let for each terminal $k \in V'$ given be the time interval $[d_k, D_k]$ during which the signal must arrive. For any intermediate vertex $i \in V\backslash V'$, we assume that $d_i = 0$ and $D_i = D = \max\limits_{k\in V'} D_k$.

Let $V_i = \{j \in V : (i,j) \in E\}$ be the set of *successors* of the vertex $i \in V$ and $i = p(j)$ be the *predecessor* of the vertex $j \in V_i$. An example of tree in a sandwich-type graph is depicted in Fig. 1. The lower level contains the root 0 and terminals 1–5. The following layers contain the intermediate vertices 6–15. The second layer is used for the interconnections parallel to the axis Oy, and the third layer, for those parallel to the axis Ox. The interlayer connections (vias))are parallel to the axis Oz. The arrows show the path $P_9(T)$ by way of example. The set $V_9 = \{8, 10\}$, for instance, is the set of successors of vertex 9, and $p(9) = 14$ is its predecessor.

We decompose the set of tree vertices into levels according to the number of arcs along the path from the root (Fig. 2). Let the number of levels be $L \le n$. We assume that the finite set X_{ij} of possible interconnection types and $\max\limits_{(i,j)\in T} |X_{ij}| = X$ are given for each arc $(i,j) \in E$. By the "interconnection type" may be meant the wire size, type of metal, and other characteristics.

As follows from the Elmor formulas (2), (3), the time of delay along the arc (i,j) depends on its capacitance and resistance, as well as on the total capacitance C_j of the subtree T_j. Additionally, the time of signal arrival to an arbitrary vertex depends also on the capacitance C_0 of the entire tree $T = T_0$. At selecting the interconnection type $x \in X_{ij}$, determined are the capacitance $c_{ij}(x)$ and resistance $r_{ij}(x)$ of the arc $(i,j) \in E$, which affects the signal propagation time along the *entire* tree.

The paper considers the problem of determining the optimal types of interconnections on the arcs of a given tree for which the signal arrives to each terminal during the given time interval and

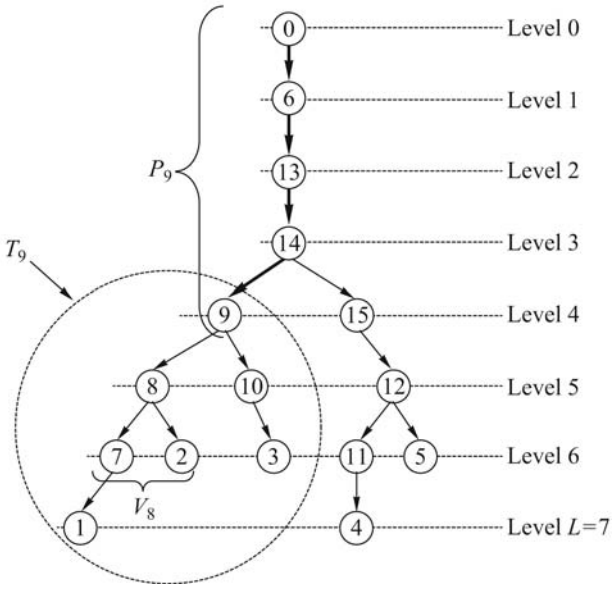

Fig. 2. Decomposition of the tree vertices to levels.

the total tree capacitance is minimal. In mathematical terms the problem is formulated as follows:

$$\sum_{(i,j)\in T} c_{ij}(x_{ij}) \to \min_{\{x_{ij}\in X_{ij}\}}; \tag{4}$$

$$t_k \in [d_k, D_k], \quad k \in V'. \tag{5}$$

The variable t_k in (5) is calculated from (3) where the capacitance $c_{ij} = c_{ij}(x)$ and resistance $r_{ij} = r_{ij}(x)$ depend on the selected interconnection type $x \in X_{ij}$ on the arc $(i, j) \in E$. At that, the delay $d_{ij}(x)$ along the arc (i, j) also depends on the interconnection type x and obeys formula (2).

Criterion (4) corresponds to minimization of the capacitance of all interconnections, which in practice leads to a reduction in the interconnection area and power dissipation. We note that the vertex capacitances are independent of the choice of interconnections and, therefore, are disregarded in the objective function.

The parameter D_k in (5) corresponds to the maximum admissible time of signal propagation from the source to the terminal k. The parameter d_k may be related with the constraint on the maximum clock skew. In particular, the conditions $t_k \geq d_k$ arise in the signal networks responsible for synchronization of the system elements. If the maximum admissible clock skew S is given, then $d_k = D_k - S$.

3. METHOD OF SOLUTION

A *one-parameter* DP scheme is suggested to solve problem (4), (5). It is applicable for *arbitrary* capacitance, $c_{ij}(x)$, and resistance, $r_{ij}(x)$, functions and any admissible time intervals $[d_k, D_k]$, $k \in V'$.

3.1. General Case

Let time assume integer values. At DP forward recursion, a conventionally optimal interconnection $x_{ij}(t)$ depending on the integer parameter t—the time of signal arrival to the predecessor vertex $i = p(j)$—is sought for each arc $(i, j) \in E$. As the result of backward recursion, the optimal solution is constructed from the conventionally optimal solution.

Forward recursion. We introduce the functional $S_{ij}(t)$ with a value corresponding to the minimum aggregate capacitance of the admissible interconnection on the arc (i,j) together with the capacitance of the subtree T_j if the signal arrives from the root to the vertex $i=p(j)$ in time t. Feasibility of interconnection on the arc (i,j) implies that all terminals of the subtree T_j receive the signal in time.

For all *leaf* terminals $j\in V'$, we calculate

$$S_{ij}(t)=\min_{x\in X_{ij}(t)} c_{ij}(x)+c_j=c_{ij}(x_{ij}(t))+c_j,\quad t=0,1,\ldots,D_j, \tag{6}$$

where $i=p(j)$, the parameter t corresponds to the time of signal arrival to the vertex i, $x_{ij}(t)$ is the conventionally optimal solution on which (6) is minimized, and $X_{ij}(t)\subseteq X_{ij}$ is a subset of admissible interconnections on the arc (i,j), that is, such that $x\in X_{ij}$, for which $d_j\le t+d_{ij}(x)\le D_j$. If no admissible interconnection $x_{ij}(t)$ exists for some t, then we assume that $S_{ij}(t)=+\infty$.

For each nonsuspended vertex i of level $L-1$ and possible values of the parameter $t\in[0,D]$, we calculate the function

$$S_i(t)=\sum_{j\in V_i} S_{ij}(t). \tag{7}$$

Let the functions $S_j(t)$ be calculated for each vertex j of the level l, $1\le l\le L-1$, and the vertex $i=p(j)$ belong to the level $l-1$. We determine values of the function

$$S_{ij}(t)=\min_{x\in X_{ij}(t)}\{c_{ij}(x)+S_j(t+d_{ij}(x))\}+c_j=c_{ij}(x_{ij}(t))+S_j(t+d_{ij}(x_{ij}(t)))+c_j, \tag{8}$$

where $X_{ij}(t)\subseteq X_{ij}$ is the subset of admissible interconnections enabling timely reception of the signal by all terminals of the subtree T_j.

Determination of the conventionally optimal solution $x_{ij}(t)$ in (8) involves difficulties associated with the peculiarities of the Elmor model. The point is that the delay along the arc (i,j) depends on the capacitance C_j of the subtree T_j. By definition, C_j corresponds to $S_j(t_j)$. As the result, the recurrent relations (8) include the recursion $S_j(t+r_{ij}(x)(c_{ij}(x)/2+S_j)$, that is, it is required to know the value of the functional S_j in order to calculate its argument.

To resolve the recursion, we consider an arbitrary interconnection x and obtain

$$S_j(t+d_{ij}(x))=S_j(t+r_{ij}(x)(c_{ij}(x)/2+S_j))=S_j(t'+r_{ij}(x)S_j)=S_j(\tau),$$

where $t'=t+r_{ij}(x)c_{ij}(x)/2$ and $\tau=t'+r_{ij}(x)S_j$. The minimum integer τ for which $r_{ij}(x)S_j(\tau)=\tau-t'$ is determined from the table of precalculated values of $S_j(\tau)$. If the desired τ does not exist, then the interconnection x is inadmissible. If no admissible interconnection exists for t, then we assume that $S_{ij}(t)=+\infty$.

Let the values of $S_{ij}(t)$ be determined for every possible value of the argument. We calculate the functional $S_i(t)$ from (7) and continue with calculating $S_{ij}(t)$ and $S_i(t)$ for the vertices of the levels with smaller numbers until $S_0(t)$ is established for every possible value of t. In the case of $S_0(t)=+\infty$, problem (4), (5) has no solution for any t. The value of t_0 is not known in advance, but by definition we get $t_0=C_0r_0$ and $C_0=S_0(t_0)=t_0/r_0$. Let us determine by enumeration of the values of $S_0(t_0)$ the minimal t_0 for which the equality $S_0(t_0)=t_0/r_0$ is true.

In the course of the forward recursion one needs to store the values of the functionals $S_{ij}(t)$ and $S_i(t)$, conventionally optimal solutions $x_{ij}(t)$, and the delay $d_{ij}(t)=d_{ij}(x_{ij}(t))$ along the arc (i,j) corresponding to the type $x_{ij}(t)$.

Backward recursion. Since the value of t_0 is known, we determine from the conventionally optimal solutions the types of optimal interconnections $x^*_{0j}=x_{0j}(t_0)$ on the arcs $(0,j)$, $j\in V_0$, and calculate

the time $t_j = t_0 + d_{0j}(t_0)$ of signal arrival to the vertex $j \in V_0$ from which we establish the optimal interconnections on the arcs connecting the vertex j with its successors. Construction of solutions for the vertices of the next levels is continued until the optimal interconnections are determined for all arcs of the tree.

In the case of integer source data, the complexity of algorithm's forward recursion is defined by the number of functionals $S_{ij}(t)$, number of possible values of the parameter t, complexity of determining the conventionally optimal solutions $x_{ij}(t)$, and values of τ for solution of the recursion. Consequently, complexity of the forward recursion is $O(nXD^2)$. The backward recursion of the algorithm is less difficult. The memory space required to store the functions $S_{ij}(t)$, $S_i(t)$, and $d_{ij}(t)$ and the conventionally optimal solutions $x_{ij}(t)$ is bounded by $O(nD)$.

3.2. Selection of Wire Size

In this section, the integer variable $x_{ij} \in X_{ij} = [a_{ij}, b_{ij}] \cap \boldsymbol{Z}$ stands for the width of interconnection along the arc $(i, j) \in E$. The capacitances and resistances of the arc are calculated from (1). The general scheme of DP is the same. At the stage of forward recursion, $S_{ij}(t)$ and the conventionally optimal solutions $x_{ij}(t)$ are calculated as before for all dangling terminals $j \in V'$. With regard for the inequalities $d_j \le t + d_{ij}(x) \le D_j$, one of the following three situations takes place.

(1) The inequality $2d_j - 2t - rcl_{ij}^2 > 0$ is satisfied and, consequently, the admissible width x satisfies

$$A_{ij}(t) = \frac{2rl_{ij}c_j}{2D_j - 2t - rcl_{ij}^2} \le x \le B_{ij}(t) = \frac{2rl_{ij}c_j}{2d_j - 2t - rcl_{ij}^2}.$$

(2) The inequalities $2d_j - 2t - rcl_{ij}^2 \le 0$ and $2D_j - 2t - rcl_{ij}^2 > 0$ are valid. Therefore, the inequality $A_{ij}(t) \le x$ must be satisfied for the admissible width.

(3) The relation $2D_j - 2t - rcl_{ij}^2 \le 0$ is true. Consequently, there is no admissible interconnection, and we assume that $S_{ij}(t) = +\infty$.

In this case, it suffices to determine the minimum integer $x \in [a_{ij}, b_{ij}] \cap [A_{ij}(t), B_{ij}(t)]$ in order to establish the conventionally optimal solution $x_{ij}(t)$. This can be done with complexity $O(\log_2(b_{ij} - a_{ij})) \le O(\log_2 X)$ using the well-known methods of one-dimensional optimization (dichotomy, for example). The function $S_{ij}(t)$ does not decrease because an increase in t leads to an increase in $A_{ij}(t)$ which may result in an increase in $x_{ij}(t)$ and, consequently, the functional $S_{ij}(t)$. The function $c_{ij}(x)$ is strictly growing, but for small variations of t the conventionally optimal solution $x(t)$ needs not to change. The functions $A_{ij}(t)$, $B_{ij}(t)$ and variables a_{ij} and b_{ij} bound the domain of values to the admissible domain $t \in [t_{\min}, t_{\max}]$ (Fig. 3). For $t \ge t_{\min}$, the functional

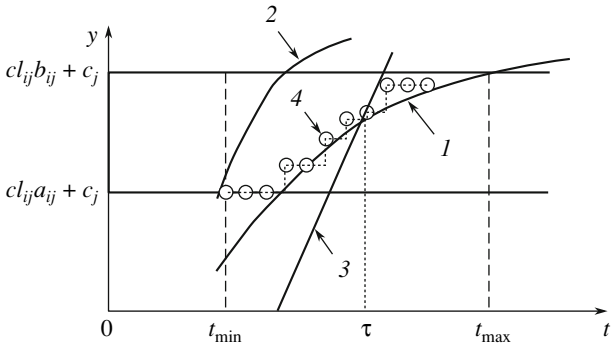

Fig. 3. Form of the Functional $y = S_{ij}(t)$. (1) $y = cl_{ij}A_{ij}(t) + c_j$; (2) $y = cl_{ij}B_{ij}(t) + c_j$; (3) $y = \frac{x}{rl_{ij}}(\tau - t) - \frac{cl_{ij}x}{2}$; (4) $y = S_{ij}(t)$.

$S_{ij}(t)$ is equal to $cl_{ij}a_{ij}+c_j$ as long as the inequality $A_{ij}(t)\le a_{ij}$ is satisfied. When at the increase of t it turns out that $A_{ij}(t)>a_{ij}$, the variable $x(t)$ increases. After that, the functional $S_{ij}(t)$ can retain its value with increasing t. Therefore, $S_{ij}(t)$ is a piecewise constant nondecreasing discrete function with the number at most $\min\{X,D\}$ steps.

For each nonsuspended vertex i of the level $L-1$, we calculate the piecewise constant function $S_i(t)=\sum\limits_{j\in V_i}S_{ij}(t)$ which has at most $|V_i|\times X$ steps and does not decrease as the sum of piecewise constant nondecreasing functions.

In virtue of relations (1), the recursion in (8) becomes as follows:

$$S_j\left(t+\frac{rl_{ij}}{x}\left(\frac{cl_{ij}x}{2}+S_j\right)\right)=S_j\left(t+\frac{rcl_{ij}^2}{2}+\frac{rl_{ij}}{x}S_j\right)=S_j(\tau).$$

Therefore, it is required to determine the minimum integer τ for which

$$S_j(\tau)=\frac{x}{rl_{ij}}(\tau-t)-\frac{cl_{ij}x}{2}. \tag{9}$$

The straight line defined by the right-hand side of (9) generally may intersect the graph of the piecewise constant function $S_j(\tau)$ more than once, though not necessarily at the integer points (Fig. 3). To determine the desired τ, it suffices to check the intersection of the line with each step (horizontal interval) of the function $S_j(\tau)$. Since the number of steps of the function $S_j(\tau)$ is bounded by Xn_j, where n_j is the number of vertices of the subtree T_j, the number of operations required is at most $O(n_jX)$.

Let us consider $S_{ij}(t)$ of (8) which is piecewise constant and nondecreasing function. The latter follows from the fact that an increase in t may lead to a right shift of the left boundary of the x-admissible interval.

If no desired τ exists for some value of x_{ij}, then the interconnection x_{ij} is not admissible for the t under consideration. If no t exists for any admissible interconnection, then we assume that $S_{ij}(t)=+\infty$.

Let the values of $S_{ij}(t)$ be established for every possible value of the argument. We calculate the functional $S_i(t)$ in (7). The functions $S_i(t)$ also are piecewise constant with the number of steps not exceeding Xn_i and nondecreasing as the sums of the piecewise constant functions. As the result, the complexity of selecting the optimal width of interconnections by the proposed algorithm is equal to $O(nXD\min\{nX,D\})$. At that, if the graph of the function $S_j(\tau)$ intersects that of the function $\dfrac{x}{rl_{ij}}(\tau-t)-\dfrac{cl_{ij}x}{2}$ at a single point τ, then the algorithm's complexity is bounded by $O(nXD\log_2 D)$.

4. PLACEMENT OF THE PLANAR TREE EDGES TO THE VLSI CIRCUIT LAYERS

The topicality of the problem considered in this section grows with the number of IC layers. If just recently an interconnection parallel say to the axis Ox inevitably got to one layer, in the today VLSI circuits there are already two or three alternatives, and the number of routing layers continues to grow from year to year.

Let us assume that on a planar (two-dimensional) lattice a projection tree $T^p=(V^p,E^p)$, $|V^p|=N$, be given. Here, an arbitrary vertex $i\in V^p$, $|V_i|\le 3$, is defined by the coordinates (x_i,y_i). Let for each arc $(i,j)\in E^p$ the set of layers P_{ij}, $1<|P_{ij}|\le$ const, where the arc can be placed be known.

In the three-dimensional space, the vertex i is defined by the triple (x_i,y_i,l), where l is the number of the layer. The placement of the arc $(i,j)\in E^p$ is specified by the number of the layer l

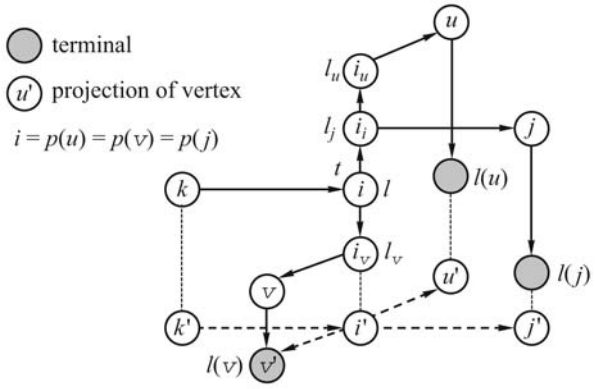

Fig. 4. Example of placement of arcs leading to the dangling terminals.

which defines the coordinates of arc beginning, (x_i, y_i, l), and end, (x_j, y_j, l). For each terminal $k \in V'$, known is the layer $l(k)$ where it is placed. Let given be the functions $a_{ij}(l)$ of the cost of placing the arc (i, j) on the layer $l \in P_{ij}$ and $a_i(l_1, l_2)$ of the cost of the vertical interconnection (via) of the vertices (x_i, y_i, l_1) and (x_i, y_i, l_2). The cost function may reflect the capacitive reactance, degree of deficit, width, or any other characteristics of the edge. The capacitance $c_{ij}(l)$ of the arc (i, j) placed on the layer $l \in P_{ij}$ and the capacitance $c_i(l_1, l_2)$ of the vertical interconnection of the vertices (x_i, y_i, l_1) and (x_i, y_i, l_2) are known as well.

It is required to place the arcs of the set E^p to the IC layers so as to minimize the total cost of interconnections and deliver signal to each terminal $k \in V'$ during the admissible time interval $[d_k,\ D_k]$.

This problem is not a special case of problem (4), (5) because it is a projection and not the tree that is given. In this connection, at determining the optimal layer for placement of the arc (i, j) it is not sufficient to known the time of signal arrival to the preceding vertex $i \in p(j) \in V^p$. The procedure of distributing the arcs of the planar tree to layers is performed using the following two-parameter dynamic programming.

Forward recursion. We introduce the function $S_i(l, t)$ of minimum cost of the subtree T_i, provided that the arc $(p(i), i)$ lies in the layer l and the signal from the source arrives to the vertex (x_i, y_i, l) in time t. The projection of the vertex v is denoted by v', and the level where it is placed, by l_v. We denote $i_v = (x_i, y_i, l_v)$, $v \in V_i$. Let first the set of successors $V_i \subseteq V^p$ of the vertex i have only leaf terminals. We consider a more complex case of $|V_i| = 3$ shown in Fig. 4 where the dashed lines show a fragment of the projection tree.

We assume that known are the layers l_s where the arcs $(i, s),\ \ s \in V_i$, are placed. Then, for the case shown in Fig. 4 we obtain

$$S_i(l, t) = a_i(l, l_v) + a_i(l, l_j) + a_i(l_j, l_u) + \sum_{s \in V_i} \left(a_{is}(l_s) + a_s(l_s, l(s))\right), \tag{10}$$

and the capacitance of the subtree T_i is equal to

$$C_i(l, t) = c_i(l, l_v) + c_i(l, l_j) + c_i(l_j, l_u) + \sum_{v \in V_i} \left(c_{iv}(l_v) + c_v(l_v, l(v)) + c_v\right).$$

We calculate the time of signal arrival to each terminal of the set V_i. For the case of Fig. 4, the time of signal arrival, for example, to the vertex j is as follows:

$$t_j = t + d_{i,i_j} + d_{i_j,j} + d_{j,j_{l(j)}}$$
$$= t + r_{i,i_j}\left(c_{i,i_j}/2 + C_{i_j}\right) + r_{i_j,j}\left(c_{i_j,j}/2 + C_j\right) + r_{j,j_{l(j)}}\left(c_{j,j_{l(j)}}/2 + c_j\right).$$

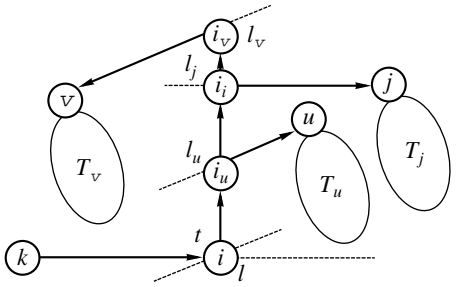

Fig. 5. Example of placement of arcs outgoing from an arbitrary vertex.

For the fixed values of the parameters l and t, we calculate the cost of the capacitance of the subtree T_i and the rime of signal arrival to all terminals of the subtree T_i for each variant of placement of the arcs (i,j), $j \in V_i$. If there is a terminal $s \in V_i$ for which $t_s \notin [d_s, D_s]$, then this arc placement is inadmissible. By enumerating every possible variant of arc placement we store the minimal cost, its corresponding capacitance of the subtree T_i, and placement itself. If there is no admissible variant of placement, then we assume that $S_i(l,t) = +\infty$.

In virtue of the condition $|P_{ij}| \le \text{const}$, the optimal placement of arcs (i,j), $j \in V_i$, is established for fixed values of the parameters l and t with complexity $O(1)$. Consequently, in the case at hand the complexity of calculating the function $S_i(l,t)$ is defined by the number of possible values of the parameter in the given t and is equal to $O(D)$.

Now, let i be an arbitrary vertex of the projection tree T^p and the functions $S_j(l,t)$ and their corresponding capacitances $C_j(l,t)$ be calculated for all its successors $j \in V_i$. We consider a more complicated case where $|V_i| = 3$ and, additionally, the levels of placement of successors are either above or below the level l. An example of such placement is shown in Fig. 5. As before, let l be the layer to which the arc $(p(i), i)$ belongs and t be the time of signal arrival to the vertex $i = (x_i, y_i, l)$. If the placement of arcs (i,s), $s \in V_i$, is known and corresponds, for example, to Fig. 5, then

$$S_i(l,t) = a_i(l,l_u) + a_i(l_u,l_j) + a_i(l_j,l_v) + \sum_{s\in V_i} \left(a_{is}(l_s) + S_s(l_s, t+t_{is})\right), \tag{11}$$

$$C_i(l,t) = c_i(l,l_u) + c_i(l_u,l_j) + c_i(l_j,l_v) + \sum_{s\in V_i} \left(c_{is}(l_s) + C_s(l_s, t+t_{is}) + c_s\right), \tag{12}$$

where

$$t_{iu} = d_{i,i_u} + d_{i_u,u}; \quad t_{ij} = d_{i,i_u} + d_{i_u,i_j} + d_{i_j,j}; \quad t_{iv} = d_{i,i_u} + d_{i_u,i_j} + d_{i_j,i_v} + d_{i_v,v};$$

$$d_{i,i_u} = r_{i,i_u}\Big(c_{i,i_u}/2 + c_{i_u,u} + C_u(l_u, t+t_{iu}) + c_{i_u,i_j} + c_{i_jj} + C_j(l_j, t+t_{ij}) + c_{i_j,i_v} + c_{i_v,v} + C_v(l_v, t+t_{iv})\Big);$$

$$d_{i_u,u} = r_{i_u,u}\left(c_{i_u,u}/2 + C_u(l_u, t+t_{iu})\right);$$

$$d_{i_u,i_j} = r_{i_u,i_j}\left(c_{i_u,i_j}/2 + c_{i_j,j} + C(l_j, t+t_{ij}) + c_{i_j,i_v} + c_{i_v,v} + C_v(l_v, t+t_{iv})\right);$$

$$d_{i_j,j} = r_{i_j,j}\left(c_{i_j,j}/2 + C_j(l_j, t+t_{ij})\right);$$

$$d_{i_j,i_v} = r_{i_j,i_v}\left(c_{i_j,i_v}/2 + c_{i_v,v} + C_v(l_v, t+t_{iv})\right);$$

$$d_{i_v,v} = r_{i_v,v}\left(c_{i_v,v}/2 + C_v(l_v, t+t_{iv})\right).$$

We assume for simplicity that the vertex i is not a terminal. Otherwise, the values corresponding to the vertical connection of the terminal i with the tree, possibly (this depends on the place of the terminal), must be added in (11) and (12) to the cost and capacitance of the subtree.

Obviously, not any set of values of t_{iu}, t_{ij}, and t_{iv} satisfies the above relations. If the value of $t_{iv} \le D - t$ is fixed, then $t_{i,i_j} = d_{i,i_u} + d_{i_u,i_j} \le t_{ij}$ is determined uniquely. If the time $t_{ij} \in [t_{i,i_j}, D-t]$

is fixed, determined is $d_{i,i_u} \le t_{iu}$, whence it follows that the time $t_{iu} \in [d_{i,i_u}, D-t]$. For the given values of the parameters l and t, we calculate for each variant of placement of the arcs (i,j), $j \in V_i$ the cost and capacitance of the subtree T_i and the times of signal arrivals to all terminals $j \in V_i$. By enumerating every possible variant we store the minimal cost and its corresponding capacitance of the subtree T_i for admissible placement of arcs and the placement itself. If for any variant of arc placement the cost of the subtree T_i is not limited, then we assume that $S_i(l,t) = +\infty$.

The complexity of determining the optimal placement of the arcs (i,s), $s \in V_i$, of the planar tree to the layers under fixed values of l and t is determined by enumerating every possible value of time t_{is}, $s \in V_i$, and is bounded by $O(D^3)$ in virtue of the inequality $|V_i| \le 3$.

By proceeding with calculation of the subtree costs and capacitances from (11) and (12), we establish $\min\limits_t S_0(l_0,t) = S_0(l_0,t_0)$. Complexity of the forward recursion is defined by the number of possible values of the parameter t, the number of vertices of the planar graph N, and complexity of determining the optimal variant of placement of the arcs outgoing from each vertex; it is equal to $O(ND^4)$.

Backward recursion. With the knowledge of the placement layer of the root l_0 and the optimal value of t_0, determined are the layers l_v, $v \in V_0$, for placement of the arcs outgoing from the root. Then, the times of signal arrivals to the vertices $v \in V_0$ are calculated. The process of determining the layers is continued for the arcs that are more distant from the root until the layers for placement of all tree arcs are determined. Complexity of the backward recursion does not exceed that of the forward recursion.

5. CONCLUSIONS

Consideration was given to the general formulations of the problems of optimization of the interconnection types on the arcs of the given tree when the time of signal arrival to each terminal is bounded both from above and below. At that, the delay is calculated from the Elmor formulas.

For the problem of minimization of the total capacitance of the given n-vertex rooted tree where the arc capacitance and resistance are defined by *arbitrary* functions depending on the type of the interconnection used, for the first time proposed was a *one-parameter* algorithm of dynamic programming of complexity $O(nXD^2)$, where D is the maximum admissible delay from the root to the terminals and X is the maximum number of types of interconnections that may be used on one edge. In a special case where the resistance and capacitance of each arc depend on the interconnection *width* and obey (1), the complexity of problem solution is bounded by $O\left(nXD\min\{nX, D\}\right)$. We note that at solution of recursion (9) the desired value of τ is determined as a point of intersection of the graphs of nondecreasing piecewise constant function and linear function. If such point is unique, then τ may be determined with complexity $O\left(\min\{X, \log_2 D\}\right)$ which allows one to reduce to $O\left(nXD\min\{X, \log_2 D\}\right)$ the complexity of problem solution. It is planned to determine the sufficient conditions for uniqueness of intersection of the graphs of the aforementioned functions.

The second problem considered in the present paper lies in determining the VLSI circuit layer for placement of each arc of the given N-vertex *planar* tree. This problem is not a special case of the preceding problem. To the best of out knowledge, the pseudopolynomial algorithm for its solution which is applicable to arbitrary functions of interconnection cost was proposed for the first time. Complexity of the algorithm is bounded by $O(ND^4)$.

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